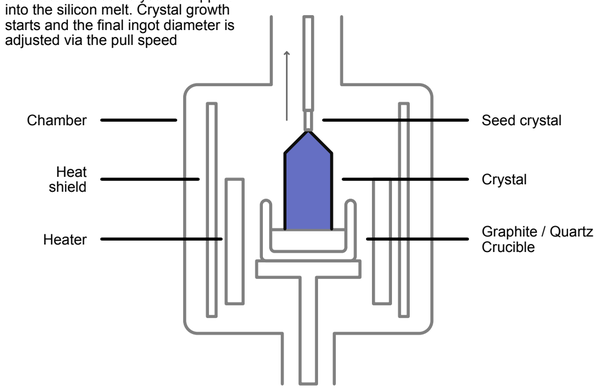
Manufacturing electronic components

The simplified process of Integrated Circuits (IC)

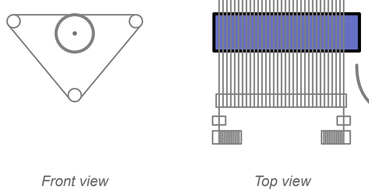
Crystal growth

Using the Czochralski Process (CZ Process) poly-silicon is melted in the crucible. The seed crystal is dipped into the silicon melt. Crystal growth starts and the final ingot diameter is adjusted via the pull speed



Wafer ingots

Wafers are sawed out of an ingot of pure crystalline silicon with diamond-coated wire. The different diameters of wafer ingots are 100 mm, 150 mm, 200 mm and 300 mm.

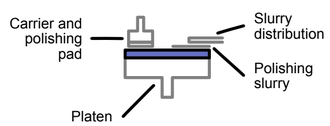


Silicon wafer

A wafer is a disk made of pure silicon. Their thickness varies according to their diameter, from 52 µm to 72 µm.

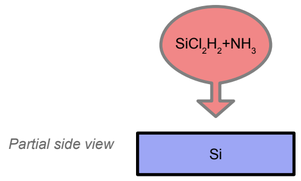
Wafer polishing

Polishing assures that the wafer surface is even and clean, removing between 5 and 10 microns of silicon. It also removes stresses and prevents warping that weakens wafers



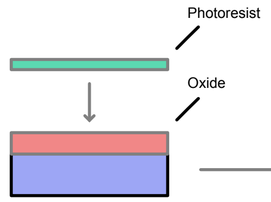
Deposition

Deposition is the fabrication process in which thin films of materials, typically an oxide, are deposited on a wafer. This layer is generally called a mask. Deposition can be physical or chemical.



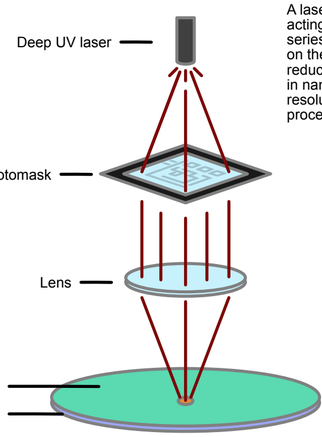
Photoresist

A photoresist, a film of protective material which is sensitive to light, is applied on top of the mask.



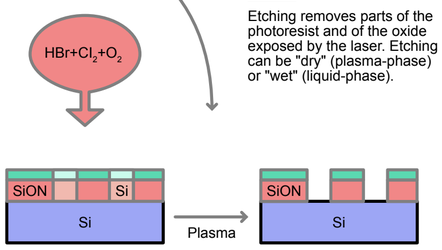
Photolithography

A laser will go through a photomask, acting like a photo negative, and a series of lenses to engrave a pattern on the photoresist. The ability to reduce the size of a node, expressed in nanometers partly depends of the resolution of the photolithography process.



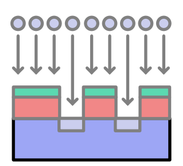
Etching

Etching removes parts of the photoresist and of the oxide exposed by the laser. Etching can be "dry" (plasma-phase) or "wet" (liquid-phase).



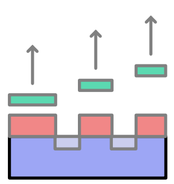
Doping

Doping introduces a small amount of charged particles, through ion implant or diffusion, on the exposed surface of the wafer to modulate its electrical properties. Dopants can be either acceptors (p-type) or donors (n-type).



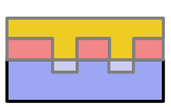
Photoresist stripping

Unwanted photoresist layers are removed from the wafer. The stripping can be "organic", "unorganic" or "dry".



Metal deposition

The back end of line (BEOL) process is perfomed to deposit the metal wiring between the transistors in order to interconnect them. BEOL process includes again photoresist, exposure to UV light and etching. BEOL adds 5 to 12 more layers.



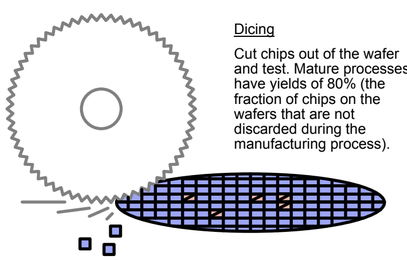
When all the layers have been deposited

Repeating

A wafer processing cycle is complete, and one layer has been fabricated. This operation will be repeated 40 to 100 times depending of the targeted number of layers.

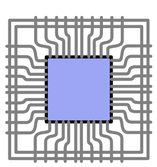
Dicing

Cut chips out of the wafer and test. Mature processes have yields of 80% (the fraction of chips on the wafers that are not discarded during the manufacturing process).



Testing and packaging

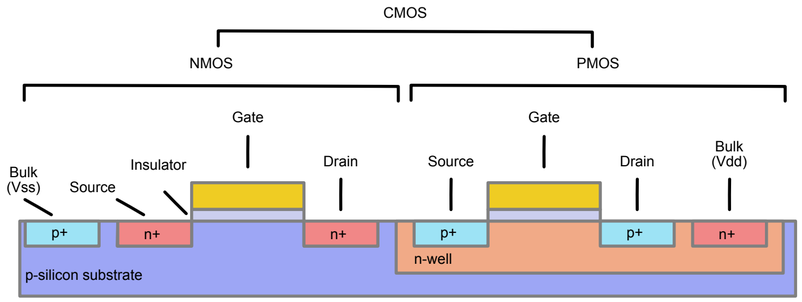
The separated chip is encapsulated in a supporting case, called package, that prevents physical damage and corrosion. The chip is then connected to the package leads. The wiring is tested to ensure that the chip has not been damaged during the packaging process.



Understanding a CMOS circuit

Partial side view

CMOS or Complementary metal-oxide-semiconductor, is a circuit composed of two transistors (PMOS, NMOS). CMOS circuits are used to create logic gates that perform logic operations.



Bulk

The bulk sets the threshold voltage of the transistor. It can be used as a ground to provide low tension, or is connected to a power supply to provide high tension.

Source

This is the part from which electrons flow.

Drain

This is the part towards which electrons flow.

Gate

By applying a tension through the gate, the flow of electrons is modified, making the transistor either conductor or insulator.

Example of a CMOS Inverter

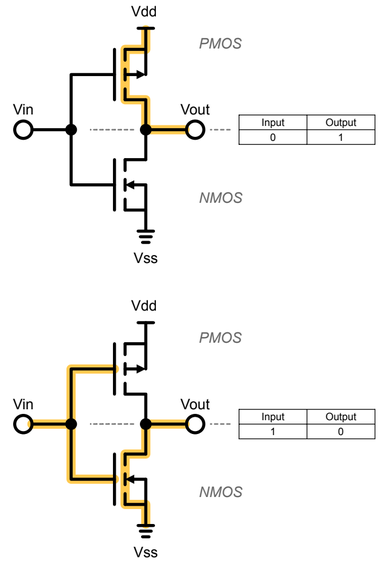
The purpose of an Inverter, or NOT gate, is to give an output, a bit in that case, opposite to the input it received, as shown on the truth table below.

Input	Output
0	1
1	0

By default, electrons flow through the PMOS transistor, from the Vdd to the Vout, due to the tension provided by the Vdd ; and electrons don't flow through the NMOS transistor.

When a tension is applied from Vin to the PMOS and NMOS gates, the flow of electrons is reversed. Electrons don't flow through the PMOS transistor anymore but flow through from the NMOS transistor to the ground, creating an electron discharge.

This is how the inverter operation is applied at an electronic level.



Sources : WikiChip, ASML

Crédits : Gauthier Roussilhe

Many thanks to Thibault Pirson from UC Louvain from his help.